REMARKS

Claims 1-8 and 10-22 are pending in this application. By this Amendment, claims 5 and 8 are amended. The amendment to claims 5 and 8 are for clarification purposes only, and not related to reasons for patentability. No new matter is added. Reconsideration and allowance of this application are respectfully requested.

CLAIM REJECTIONS - 35 U.S.C. § 112

Claims 1-5 and 5-8 stand rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

In regard to claims 5 and 8, Applicants submit that claims 5 and 8 have been amended to obviate the rejection. Specifically, claims 5 and 8 have been amended to replace "insulating interlayer" to "second insulating layer", in order to provide consistency with claim 1.

In regard to claim 1, the Examiner asserts that the term "first metal *thickness*" to be unclear. Applicants submit that the *thickness* of the metal wire 122 commences at the lower surface of first layer 120 up to the lower layer of 124a of the second layer 124 which is asserted throughout prosecution by the Applicants. For instance, paragraph [0049] discloses:

> a first metal wire 122 has a thickness which is identical of that of the capacitor 132; and
>
> the depth of the second metal contact hole 134c will be substantially identical to the height of capacitor 132 + the thickness of the upper electrode 130 + the interval between the upper electrode 130 and the first metal wiring 122 – the thickness of the first metal wiring 122.

According to the above passages, one of ordinary skill in the art will recognize that "thickness" of the metal wire is in the Y-direction (e.g., depth).

Accordingly, reconsideration and withdrawal of the rejections are respectfully requested.

CLAIM REJECTIONS - 35 U.S.C. §103

Claims 1-2 and 5-8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Okumura et al. ("Okumura"), U.S. Patent no. 6,163,046 in view of Suwanai et al. ("Suwanai"), U.S. Patent no. 5,389,558. This rejection is respectfully traversed.

Applicants submit that Okumura and Suwanai, individually or in combination, fail to disclose or suggest, *inter alia*, the "second insulating layer includes a first sub-layer surrounding the first metal wiring and a second sub-layer formed on the capacitor, the first metal wiring and the first sub-layer, the second sub-layer including a lower layer that is formed between the upper electrode and the first metal wiring, and an upper layer that is formed over the upper electrode", as recited in claim 1.

As shown in an example embodiment of the present invention, Fig. 2 illustrates a second insulating layer (120 and 124) having a first sub-layer 120 and a second sub-layer 124. The first sub-layer 120 surrounds a first metal wiring 122, and the second sub-layer 124 is formed *on* a capacitor 132, the first metal wiring 122 and the first sub-layer 120. The second sub-layer 124 further includes a lower layer 124a that is formed between an upper electrode 130 and the first metal wiring 122, and an upper layer 124b that is formed over the upper electrode 130.

The Examiner alleges that the interlayer insulating film 20 (second insulating layer) includes "a first sub-section (the lower part of second insulating layer 20) surrounding the first metal wiring 21B and a second sub-section (the upper part of second insulating layer 20) formed on the capacitor 19, the first metal wiring 20a (see Fig. 38) and the first sub-layer 14"[1]. However, it is submitted that the second sub-layer 20 of Okumura, even with the Examiner's interpretation, fails to teach or suggest that the second sub-layer is formed **on**

[1] See Final Office Action dated January 23, 2006, page 3.

the first metal wiring. Instead, Okumura discloses that the interlayer insulating film 20 (second insulating layer) surrounds the buried layer 27 (first metal wiring) (e.g., formed within the insulating interlayer 20). See Fig. 10b of Okumura.

Further, because Okumura does not disclose the second sub-layer formed on the first metal wiring, Okumura cannot teach or suggest "a lower layer that is formed between the upper electrode and the first metal wiring", as recited in claim 1.

Accordingly, Okumura, singly or in combination with Suwanai, fails to teach or suggest each feature recited in claim 1.

Moreover, the Examiner admits that Okumura fails to disclose or suggest the second sub-layer having "a lower layer" and "an upper layer", as recited in claim 1. The Examiner attempts to overcome the admitted deficiency of Okumura by arguing that Suwanai teaches the multi-layered second sub-layer.

Applicants submit that there is no motivation to combine the teachings of Suwanai with the teachings of Okumura with any expectation of success, at least, because one would have to substantially alter the reference of Suwanai to teach the combination. That is, employing a capacitor in the region of the memory cell area of Suwanai would increase the number of lithography processes and form metal contacts having greater depth in the semiconductor device.

Accordingly, one of ordinary skill in the art would not have been motivated to select the references and to combine them to render the claimed invention obvious, In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the Examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

Thus, the Examiner has not adequately supported the selection and combination of Okumura and Suwanai to render obvious that which Applicants have claimed. The Examiner's conclusory statement that "[i]t would be obvious to a person of ordinary skill in the art at the time

the invention was made to use a second insulating layer which includes a first sub-layer and a second sub-layer, wherein the second sub-layer including a lower layer and an upper layer in Okumura et al.'s device in order to improve the protection to the device by having a plurality of layers"[2], does not adequately address the issue of motivation to combine. This factual question of motivation is material to patentability, and can not be resolved on subjective belief and unknown authority. It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to "[use] that which the inventor taught against its teacher." W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983). The Examiner must explain the reasoning behind his findings of motivation. Simply stating that the motivation for combining Okumura and Suwanai "to improve the protection to the device" is an insufficient explanation for the alleged combination.

Further, Applicant submits that combining the teachings of Suwanai with the teachings of Okumura is use of *impermissible hindsight* reconstruction to reject the claims. The Examiner has used the present application as a blueprint, selected a prior art semiconductor device in Okumura as the main structure, and then searched other prior art for the missing elements (e.g., multi-layer second insulating layer), without identifying or discussing any specific evidence of motivation to combine, other than providing conclusory statements regarding the knowledge in the art, motivation and obviousness. The Federal Circuit has noted that the PTO and the courts "cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention," In re Fine, 837 F.2d 1071, 1075, 5 USPQ2d 1780, 1783 (Fed. Cir. 1988), and that the best defense against hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references. Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight. Dembiczak, 50 USPQ2d at 1617.

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[2] See Final Office Action dated January 23, 2006, page 4.

Accordingly, for at least these reasons, claim 1 and those claims dependent thereon are allowable over the applied art. Withdrawal of the rejection is respectfully requested.

RESPONSE TO ARGUMENTS

The Examiner asserts in the "Response to Arguments" that:

> in claim 1, Applicant arbitrarily categorizes layers 120, 1204a and 124b as one layer (second insulated layer), which can be divided into three separate sections (layers). Applying the same analogy to prior art, Okumura et al. teaches one layer (second insulating layer 20) which can be arbitrarily be divided into three sections (layers) (*emphasis added*).

However, it is submitted that the second insulating layer 120 and 124 are not arbitrarily formed, as suggested by the Examiner. The second insulating layer 120 and 124 are three distinct identifying structures formed by different decomposition processes to reflect the construction of the semiconductor device (*see* Figs. 3B - 3E and paragraphs [0041] - [0046] in the instant disclosure for support). Thus, it is submitted that Applicants are not arbitrarily categorizing layers 120, 124a and 124b as one layer which can be divided into three separate sections, as asserted by the Examiner.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the rejections and allowance of each of the claims in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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